Triggering a Current Controlled Solidtron (CCS) Device

Introduction

Best practices in the design of solid state initiator circuits yield waveforms with a high di/dt, minimum turn-on delay, and low jitter. The trigger circuit for CCS devices plays an important role in mitigating turn-on delay and jitter. To do so, CCS devices should be triggered in a way that minimizes the amount of time the gate of the CCS spends between its off-state bias and its Turn-on gate threshold voltage (V_{GT}). The following describes a simple way to investigate the performance of the end user's gate drive.

The gate input of all CCS products can be represented as a p-n junction diode. To turn the CCS device on, the representative diode must be forward biased. Like any p-n diode, this diode has an associated junction capacitance. Using this model, this capacitance must be charged to the diode's forward biasing voltage to initiate turn-on of the CCS device.

Simulation

A simple way to predict the performance of a gate drive with a CCS part is to use a discrete based model as shown in Figure 1. In this model an ideal diode (Gate-diode) in parallel with a capacitor (Gate-capacitance) represent the gate input of a CCS device. R-off is a keep off resistor utilized to sink leakage and dV/dt current to prevent unwanted turn-on. L-stray represents the inductance between the gate terminal and keep off resistor. Here, a 1A peak sine wave with a 1µs wide ½-pulse-width is used to trigger the gate.

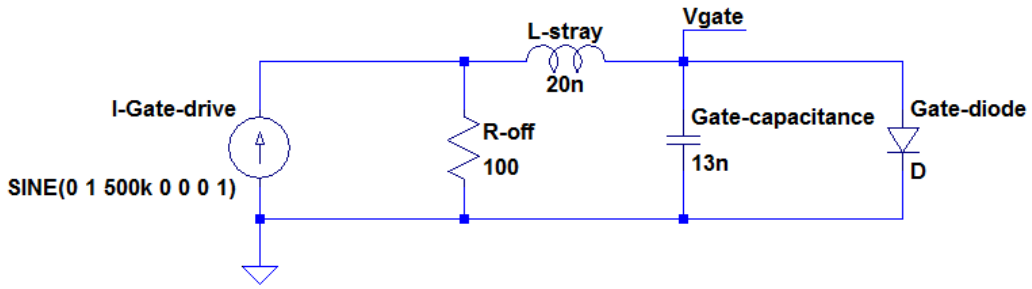

Figure 1 Discrete-based model of CCS gate input and gate drive

This simplified model demonstrates the order of operation during turn-on of CCS devices by ignoring the more complicated features of p-n junction physics. Figure 2 demonstrates the division of current between the keep off resistor, the gate capacitance, and the junction itself.

An important note to make is that this model is for instructional purposes only. The value of gate capacitance is a function of the specific Solidtron part number. The forward bias voltage of the diode used in this model is 800mV, while the V_{GT} of CCS devices is closer to 500mV (25°C)

Plot Definitions

From top to bottom, Figure 2 depicts the gate terminal's voltage, V(vgate); the gate capacitor current, I(Gate-capacitance) and gate diode current, I(Gate-diode); the keep-off resistor current I(R-off); and the gate drive supply current, I(I-gate-drive).

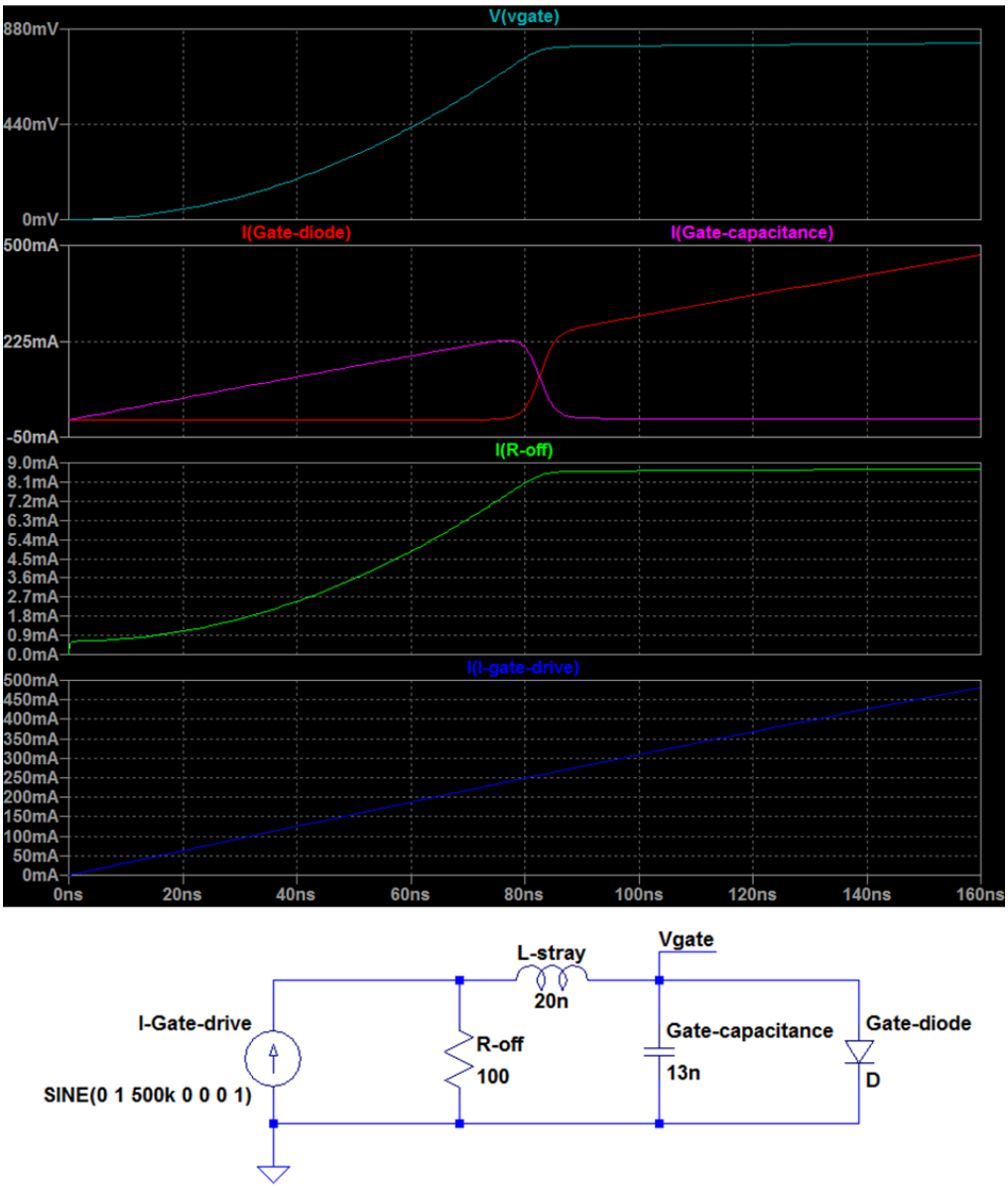

Figure 2 Simulation results of discrete-based model

Theory of Operation

At t=0, the trigger voltage is applied to the circuit. First, L-stray develops a voltage across it as a function of L*di/dt, causing the initial steep slope in I(R-off). As current flows into the gate terminal the gate capacitance begins to charge; however, the diode does not forward bias until the terminal voltage (vgate) approaches 800mV, forward biasing threshold of Gate-diode. At t ≅ 80ns, vgate reaches the forward biasing threshold. At this point, current flows into Gate-diode initiating the turn-on sequence.